CLAIMS

What is claimed is:

1. A method of implementing a user circuit in a programmable logic device (PLD), comprising:

selecting a first logical grouping from the user circuit based on cost criteria;

selecting a second logical grouping from the user circuit based on the cost criteria; and

generating a configuration data file enabling a first level of well biasing for the first logical grouping and a second level of well biasing for the second logical grouping.

2. The method of Claim 1, wherein:

the first level of well biasing is a positive well bias; and

the second level of well biasing is no applied well bias.

3. The method of Claim 1, wherein:

the first level of well biasing is a negative well bias; and

the second level of well biasing is no applied well bias.

4. The method of Claim 1, wherein:

the first level of well biasing is a positive well bias; and

the second level of well biasing is a negative well bias.

5. The method of Claim 1, wherein:

the first and second levels of well biasing are of the same polarity but different values.

6. The method of Claim 1, wherein the cost criteria include the performance of the first logical grouping.

7. The method of Claim 1, wherein the cost criteria include the power consumption of the user circuit.

8. The method of Claim 1, wherein the second logic grouping comprises all portions of the user circuit not included in the first logical grouping.

9. A method of implementing a user circuit in a programmable logic device (PLD), comprising:

determining a first set of transistors on a first critical path in the user circuit;

designating the first set of transistors as critical path transistors; and

generating a configuration data file enabling positive well biasing of the critical path transistors.

10. The method of Claim 9, further comprising prior to generating the configuration data file:

determining a second set of transistors on a second critical path in the user circuit; and

designating the second set of transistors as critical path transistors.

11. The method of Claim 10, further comprising:

monitoring a number of the transistors designated as critical path transistors; and

issuing an error message if the number of the transistors designated as critical path transistors exceeds a pre-established maximum.

12. The method of Claim 9, wherein determining the first set of transistors on a first critical path in the user circuit comprises accepting critical path information from the user.

13. The method of Claim 9, wherein determining the first set of transistors on a first critical path in the user circuit comprises:

calculating delays on a plurality of paths through the user circuit; and

comparing the delays to determine a slowest path through the circuit.

14. The method of Claim 9, further comprising:

determining a third set of transistors on a first non-critical path in the user circuit;

designating the third set of transistors as non-critical path transistors; and

including in the configuration data file bits that enable negative well biasing of the non-critical path transistors.

15. The method of Claim 9, further comprising:

determining a third set of transistors on a first non-critical path in the user circuit;

designating the third set of transistors as non-critical path transistors;

monitoring a number of transistors designated as critical path transistors; and

including in the configuration data file, if the number of transistors designated as critical path transistors exceeds a pre-established maximum, bits that enable negative well biasing of the non-critical path transistors.

16. The method of Claim 9, wherein:

the PLD is a field programmable gate array (FPGA); and

the configuration data file is an FPGA bitstream.

17. A method of implementing a user circuit in a programmable logic device (PLD), comprising:

determining a first set of transistors on a first non-critical path in the user circuit;

designating the first set of transistors as non-critical path transistors; and

generating a configuration data file enabling negative well biasing of the non-critical path transistors.

18. The method of Claim 17, wherein determining the first set of transistors on a first non-critical path in the user circuit comprises accepting non-critical path information from the user.

19. The method of Claim 17, wherein determining the first set of transistors on a first non-critical path in the user circuit comprises:

calculating delays on a plurality of paths through the user circuit; and

comparing the delays to determine a fastest path through the circuit.

20. The method of Claim 17, wherein:

the PLD is a field programmable gate array (FPGA); and

the configuration data file is an FPGA bitstream.

21. A method of implementing a user circuit in a programmable logic device (PLD), comprising:

evaluating the user circuit to determine timing delays on first and second paths through the user circuit;

comparing the timing delays to determine a faster path and a slower path of the first and second paths; and

generating a configuration data file selectively enabling well biasing for one or more transistors on at least one of the faster and slower paths.

22. The method of Claim 21, wherein the configuration data file enables positive well biasing for one or more transistors on the slower path.

23. The method of Claim 22, wherein the configuration data file further enables negative well biasing for one or more transistors on the faster path.

24. The method of Claim 21, wherein the configuration data file enables negative well biasing for one or more transistors on the faster path.

25. The method of Claim 21, further comprising:

determining a difference between the timing delays of the slowest and fastest paths;

determining, based on the difference between the timing delays, a preferred positive well bias value for a first transistor on the slower path, the preferred positive well bias value being one of a plurality of supported positive well bias values; and

including in the configuration data file information selecting the preferred positive well bias value for application to the first transistor.

26. The method of Claim 21, wherein the preferred positive well bias value is the smallest of the supported positive well bias values that is sufficient to make the timing delay of the slower path about the same as the timing delay of the faster path.

27. The method of Claim 21, wherein the plurality of supported positive well bias values comprises 0 volts, +X/3 volts, +2X/3 volts, and +X volts, where X is a positive value.

28. A method of implementing a user circuit in a programmable logic device (PLD), the user circuit having a plurality of paths therethrough, the PLD comprising a plurality of transistors, the method comprising:

evaluating the user circuit to determine timing delays on first and second paths through the user circuit;

determining a difference between the timing delays of the first and second paths;

evaluating the first and second paths to determine which of the transistors are included in each path;

determining, based on the difference between the timing delays and the path on which each transistor lies, a preferred well bias value for each of one or more transistors on the first and second paths, the preferred well bias value for each transistor being one of a plurality of supported well bias values; and

generating a configuration data file selecting the preferred well bias value for each of the one or more transistors.